CLAIMS

What is claimed is:

1. An oscillator (200) comprising: a first resistor (R1), a second resistor (R2), and a capacitor (C), wherein an oscillation frequency of the oscillator (200) is dependent upon a difference between a first resistance value of the first resistor (R1) and a second resistance value of the second resistor (R2), the first resistance value being larger than the second resistance value, the first resistor (R1) exhibits a first rate of change with temperature, and the second resistor (R2) exhibits a second rate of change with temperature that is larger than the first rate of change, thereby allowing temperature-induced changes to the first resistance value to be offset by changes to the second resistance value, and thereby reducing variations in the oscillation frequency with temperature.

2. An oscillator (200) as claimed in claim 1, comprising: a first stage (150a-R1-160a), operably coupled to the first resistor (R1), that is configured to provide a first voltage level, based on the first resistance value, a second stage (150c-R2-160c), operably coupled to the second resistor (R2), that is configured to provide a second voltage level, based on the second resistance value, and a switching stage (110-130, 170), operably coupled to the first stage (150a-R1-160a), the second stage (150c-R2-160c), and the capacitor (C), and is configured to: decrease a voltage on the capacitor (C) when the voltage increases to the first voltage level, increase the voltage on the capacitor (C) when the voltage decreases to the second voltage level.

3. The oscillator (200) of claim 2, wherein the first resistor (R1) substantially controls current flows through the first stage (150a-R1-160a), the second stage (150c-R2-160c), and the capacitor (C).

4. The oscillator (200) of claim 3, wherein the current flows through the first stage (150a-R1-160a), the second stage (150c-R2-160c), and the capacitor (C) are substantially equal in magnitude.

5. The oscillator (200) of claim 4, wherein the second resistance value is selected based on the first resistance value, the first rate of change, and the second rate of change.

6. The oscillator (200) of claim 5, wherein the second resistance value is selected based also on a delay associated with a feedback loop of the oscillator (200).

7. The oscillator (200) of claim 5, wherein a value of the second resistance value at a base temperature includes a factor of $R_d*(K1/(K2-K1))$, and a value of the first

resistance value at the base temperature is substantially equal to R_d plus the value of the second resistance value at the base temperature, where R_d corresponds to the difference between the first resistance value and the second resistance value at a base temperature, K1 is the first rate of change, and K2 is the second rate of change.

8. The oscillator (200) of claim 7, wherein the value of the second resistance value at the base temperature further includes a second factor of (D/C)*((Kd-K1)/(K2-K1)), where D is a delay associated with a feedback loop of the oscillator (200) at the base temperature, C is a capacitance value of the capacitor (C), and Kd is a rate of change of the delay with temperature.

9. The oscillator (200) of claim 1, wherein the first resistor (R1) is formed as a Ppoly resistor of a CMOS device, and the second resistor (R2) is formed as an Nwell resistor of the CMOS device.

10. An oscillator (200) comprising: a first stage (150a-R1-160a) that includes: a diode-configured Pchannel device (150a) operably coupled to a first voltage source, a diode-configured Nchannel device (160a) operably coupled to a second voltage source, and a first resistor (R1) operably coupled in series between the diode-configured Pchannel (150a) and Nchannel (160a) devices, a first voltage level being provided at a first node that couples the first resistor (R1) to the diode-configured Pchannel device (150a), a second stage (150c-R2-160c) that includes a Pchannel device (150c) operably coupled to the first voltage source and having a gate that is common to the first node, a diode-connected Nchannel device (160c) operably coupled to the second voltage source, and a second resistor (R2) operably coupled in series between the Pchannel device (150c) and the diode-configured Nchannel device (160c) of the second stage (150c-R2-160c), a second voltage level being provided at a second node that couples the second resistor (R2) to the Pchannel device (150c); a switching stage (110-130, 170) that is configured to control a voltage on a capacitor (C) such that: the voltage is decreased when the voltage increases to the first voltage level, and the voltage is increased when the voltage decreases to the second voltage level.

11. The oscillator (200) of claim 10, wherein the first resistor (R1) has a first temperature coefficient, and the second resistor (R2) has a second temperature coefficient that is substantially larger than the first temperature coefficient.

12. The oscillator (200) of claim 11, wherein a reference voltage is provided at a reference node that couples the first resistor (R1) to the diode-configured Nchannel device

(160a) of the first stage (150a-R1-160a), and the switching stage (110-130, 170) includes a Pchannel device (150b) operably coupled to the first voltage source and having a gate that is common to the first node, an Nchannel device (160b) operably coupled to the second voltage source, and having a gate that is common to the reference node, wherein the switching stage (110-130, 170) is configured to couple the capacitor (C) to the Pchannel device (150b) of the switching stage (110-130, 170) to increase the voltage on the capacitor (C), and couple the capacitor (C) to the Nchannel device (160b) of the switching stage (110-130, 170) to decrease the voltage on the capacitor (C).

13. The oscillator (200) of claim 12, wherein the switching stage (110-130, 170) includes: a first comparator (110) that is configured to compare the voltage on the capacitor (C) to the first voltage level, a second comparator (120) that is configured to compare the voltage on the capacitor (C) to the second voltage level, and a bistable device (130) that is configured to control the coupling of the capacitor (C) to the Pchannel device (150b) and Nchannel device (160b) of the switching stage (110-130, 170), based on an output of the first comparator (110) and an output of the second comparator (120).

14. The oscillator (200) of claim 10, wherein a reference voltage is provided at a reference node that couples the first resistor (R1) to the diode-configured Nchannel device (160a) of the first stage (150a-R1-160a), and the switching stage (110-130, 170) includes a Pchannel device (150b) operably coupled to the first voltage source and having a gate that is common to the first node, an Nchannel device (160b) operably coupled to the second voltage source, and having a gate that is common to the reference node, wherein the switching stage (110-130, 170) is configured to couple the capacitor (C) to the Pchannel device (150b) of the switching stage (110-130, 170) to increase the voltage on the capacitor (C), and couple the capacitor (C) to the Nchannel device (160b) of the switching stage (110-130, 170) to decrease the voltage on the capacitor (C).

15. The oscillator (200) of claim 14, wherein the switching stage (110-130, 170) includes: a first comparator (110) that is configured to compare the voltage on the capacitor (C) to the first voltage level, a second comparator (120) that is configured to compare the voltage on the capacitor (C) to the second voltage level, and a bistable device (130) that is configured to control the coupling of the capacitor (C) to the Pchannel device (150b) and Nchannel device (160b) of the switching stage (110-130, 170), based on an output of the first comparator (110) and an output of the second comparator (120).

16. The oscillator (200) of claim 10, wherein the switching stage (110-130, 170) includes: a first comparator (110) that is configured to compare the voltage on the capacitor (C) to the first voltage level, a second comparator (120) that is configured to compare the voltage on the capacitor (C) to the second voltage level, and a bistable device (130) that is configured to control a direction of current applied to the capacitor (C) to increase or decrease the voltage on the capacitor (C), based on an output of the first comparator (110) and an output of the second comparator (120).

17. The oscillator (200) of claim 10, wherein the first resistor (R1) is formed as a Ppoly resistor, and the second resistor (R2) is formed as an Nwell resistor.